Module Introduction

PURPOSE:

- This module, ColdFire Application-specific Peripherals, provides an overview of the relationship between ColdFire and various application-specific peripherals. The intent is to provide a baseline of knowledge related to the ColdFire processor product line's integration.

OBJECTIVES:

- Identify the features of the components of the System Control Module (SCM).
- Identify the features and functions of the Edge Port (EPORT) module.
- Identify the features and functions of the RAM Dual Port Processor.
- Examine the attributes and operation of the Programmable Interrupt Timer (PIT).
- Identify the features of the Queued Analog-to-Digital Converter (QADC) module.
- Identify the features and functions of the Watchdog Timer.
- Identify the features of the FlexCAN module.
- Identify the features of the ColdFire Flash Module (CFM).
- Identify the features of the General Purpose (GP) timers of ColdFire.

CONTENT:

- 25 pages
- 4 questions

LEARNING TIME:

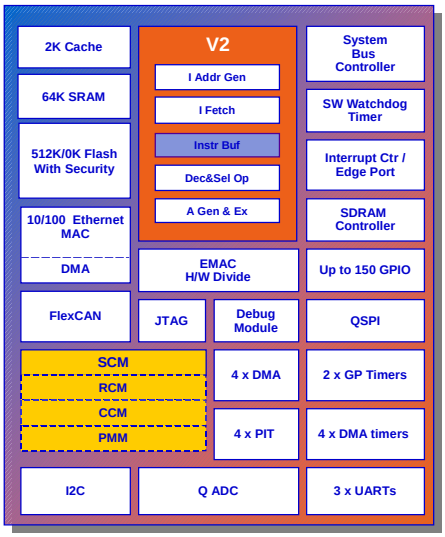
- 40 minutes

This module, ColdFire Application Specific Peripherals, provides an overview of the relationship between ColdFire and various application-specific peripherals. The intent is to provide a baseline of knowledge related to the ColdFire processor product line's integration.

In this module, you will learn the features and operation of the following modules: the System Control Module (SCM), the Edge Port (EPORT) module, the RAM Dual Port Processor, the Programmable Interrupt Timer (PIT), the Queued Analog to Digital Converter Module (QADC), Watchdog Timer, the FlexCAN module, the ColdFire Flash Module (CFM), and the General Purpose (GP) timers of ColdFire.

System Control Module

- **Consists of the Reset Control Module (RCM), Chip Configuration Module (CCM), Power Management Module (PMM), and other system control functions**
- **Provides capability to configure the system to operate in one of multiple functional modes.**
- **Provides the user the capability to control and track all sources capable of generating a reset within the system.**
- **Provides 7 sources of reset and indication of last reset**
- **Provides low power mode configuration and entry**



The System Control Module (SCM) is composed of three main blocks: the Reset Control Module (RCM), Chip Configuration Module (CCM), and Power Management Module (PMM).

It also provides the user with the capability to configure the system to operate in one of multiple functional modes.

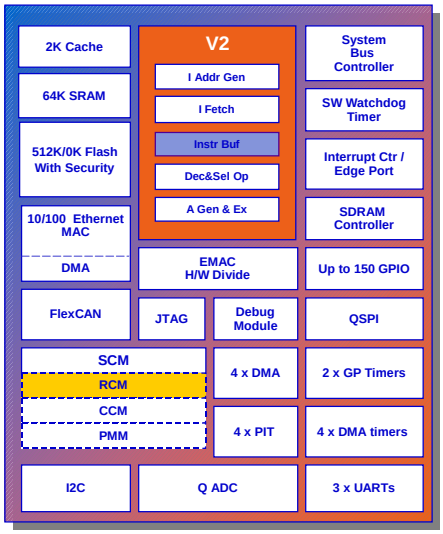
It provides the user the capability to control and track all sources capable of generating a reset within the system.

It also provides the user with seven sources of reset and an indication of last reset that has taken place.

Finally, this module allows for configuration of, and entry into, a number of low power modes.

Reset Controller Module (RCM)

- **Determines the cause of reset**
- **Asserts the appropriate reset signals to the system**
- **Keeps a history of the cause of the reset**
- **Seven Sources of Reset**
  - **External (reset pin)**
  - **Power on Reset (POR)**
  - **Watchdog Timer**
  - **PLL loss of clock**
  - **PLL loss of lock**
  - **Software**
  - **Low Voltage Detection (LVD)**

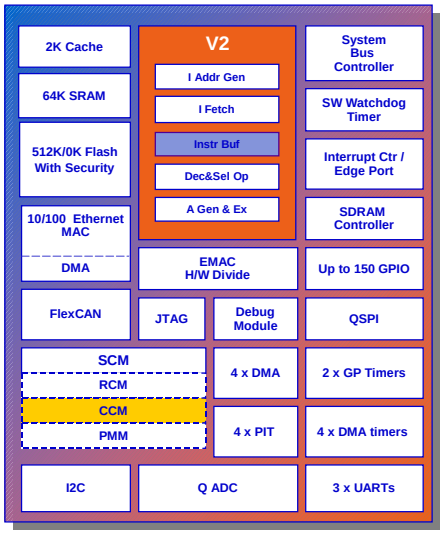


Now we'll examine the Reset Controller Module (RCM). The RCM is provided to determine the cause of reset, assert the appropriate reset signals to the system, and then to keep a history of what caused the reset. The Power Management Module (PMM) control registers are implemented in the RCM. These registers mainly control the operation of the Low Voltage Detect (LVD) circuit.

There are seven sources of reset in the RCM. They include external (reset pin), Power on Reset (POR), watchdog timer, PLL loss of clock, PLL loss of lock, software, and LVD.

Chip Configuration Module (CCM)

- **Selects Operating Mode**
  - **Master Mode**
  - **Single Chip Mode**
- **Selects PLL Mode**
  - **External Clock Mode**
  - **1:1 PLL Mode**
  - **Normal PLL Mode (x2 to x9 multiply options)**
- **Selects Boot Device**
  - **Internal (32-bit)**
  - **External (32-bit, 16-bit, or 8-bit)**
- **Selects Output Pad Drive Strength**
  - **Full Strength**
  - **Partial Strength**
- **Selects Chip Select Configuration**
  - **A[23:21] or CS[6:4]**



The Chip Configuration Module (CCM) controls chip configuration and low power mode operation.

The CCM configures the chip for two modes of operation: master mode and single-chip mode. The operating mode is determined at reset and cannot be changed thereafter. In master mode, the internal ColdFire CPU can access external memories and peripherals. Full master mode functionality is supported by the external interface module, which includes the external address bus, chip selects, and other bus control signals. The external bus consists of a 32-bit data bus configurable as an 8, 16 or 32-bit data width, and 24 address lines. In single-chip mode, all memory is internal to the chip. External bus pins are configured as general-purpose digital I/O.

The CCM selects the clock operation. This gives customers the option of using an External Clock or Phased-Lock Loop (PLL) mode with reference type being either a crystal or clock.

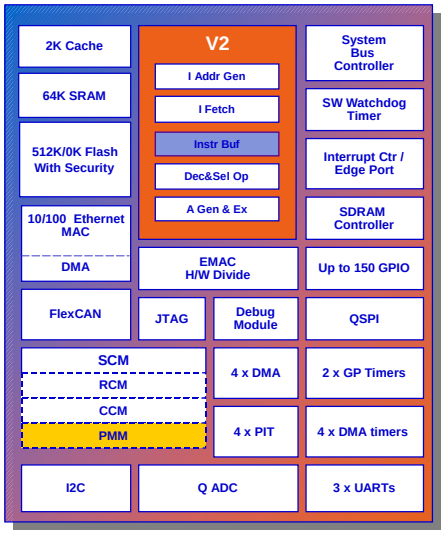
The CCM also selects the boot device. This allows the user to have the option of booting internally or externally.

The CCM can also select the output pad strength. This allows the user to either use the default pad strength or the full pad strength.

It also controls the chip select configuration. The default function of the chip select configuration can be overridden during reset configuration.

Power Management Module (PMM)

- **Controls the low power operation**
- **Four modes of operation: Run, Wait, Doze, and Stop**
- **Most peripherals can be shutdown independently**



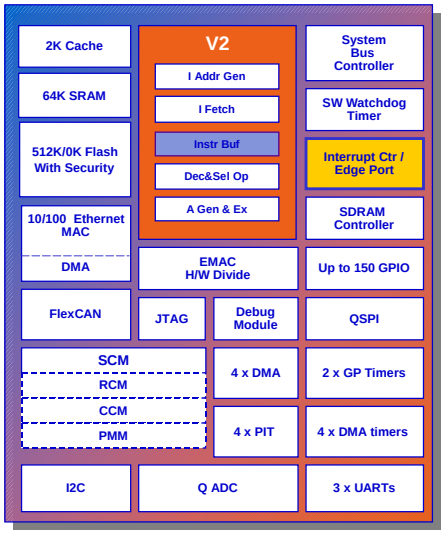
The Power Management Module (PMM) controls the low power operation on the MCF5282.

The PMM has four modes of operation: run, wait, doze, and stop. The run mode is the normal system operating mode where current consumption is related directly to the system clock frequency. The wait mode is intended to be used to stop only the CPU and memory clocks until a wakeup event is detected. The doze mode affects the CPU in the same manner as wait mode, except that each peripheral defines individual operation characteristics in doze mode. Finally, the stop mode affects the CPU in the same manner as wait and doze, with the exception that all clocks to the system are stopped and the peripherals cease operation.

The stop mode also gives the user the ability to shut down most peripherals independently including the external CLKOUT pin.

EPORT

- **Pins can used for either:**
  - **Interrupts**
  - **GPIO**
- **Supports eight sources of external interrupts**
- **Interrupt Sensitivity**
  - **Edge Sensitivity**
  - **Low-Level Sensitivity**
- **Edge Sensitivity**
  - **Rising edge**
  - **Falling edge**
  - **Both**
- **Schmitt-triggers reduce false interrupts**
- **Operates in all three low-power modes.**

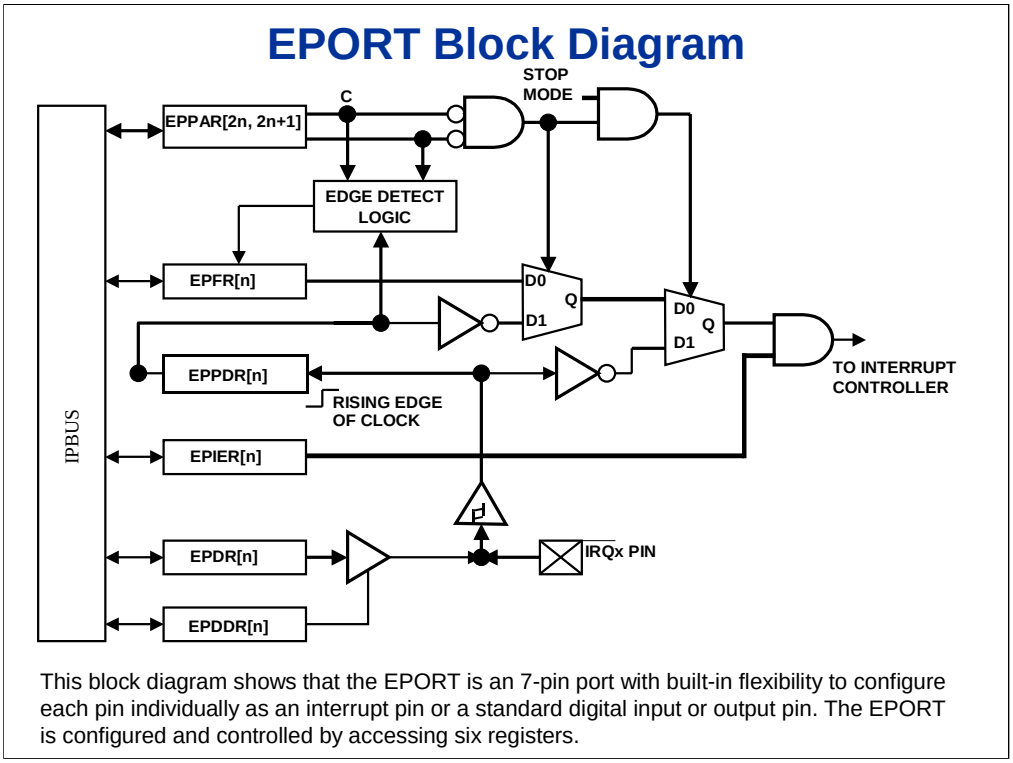


The Edge Port (EPORT) on the MCF5282 is a collection of seven pins that can be used as interrupt pins or GPIO pins.

When used as an external interrupt each of the seven pins can be individually configured for low-level sensitivity or edge-detecting sensitivity. When edge sensitivity is selected, the edge can be specified as rising edge, falling edge or both edges.

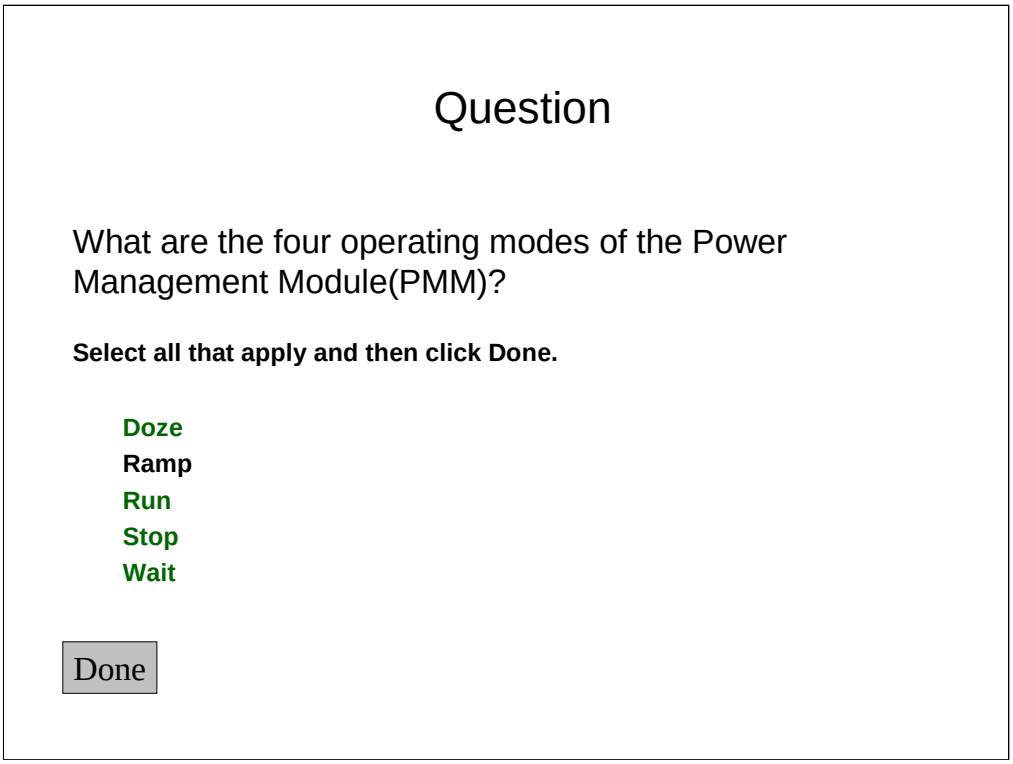
Alternatively, the pin's interrupt capability can be disabled, turning the pin into a General-Purpose I/O (GPIO) pin. Schmitt trigger logic has been incorporated into the port design so that, when configured for edge sensitivity, false interrupts are avoided on slow rise/fall time transitions.

The EPORT is totally functional in either DOZE or WAIT modes of low-power operation, and in fact can be used to bring the processor out of either mode. The same is true in STOP mode except that, since all internal clocks are disabled, the EPORT loses the capability to sync on edge-triggered interrupts and thus only level-sensitive interrupts can be sensed in this mode of operation.



This block diagram shows that the EPORT is an 7-pin port with built-in flexibility to configure each pin individually as an interrupt pin or a standard digital input or output pin. The EPORT is configured and controlled by accessing six registers.

[Reference material for previous page]



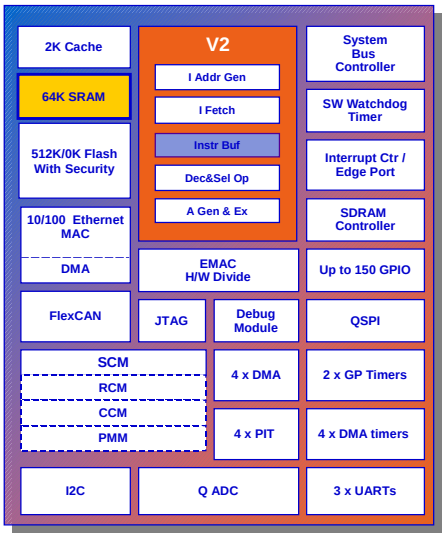
Here’s a question to test your comprehension of the material presented so far.

Answer:

The PMM has four modes of operation: run, wait, doze, and stop.

SRAM

- **RAM uses two single port arrays and a two-way banked access scheme**
- **Creates a second port to the RAM memory**
- **Manages the dual port memory resource**

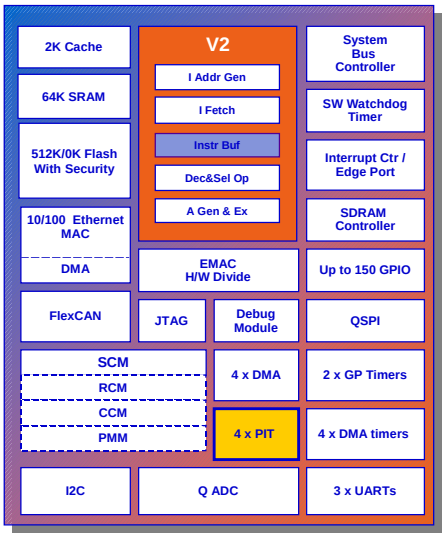


Many of the current ColdFire designs and future ColdFire design opportunities involve the processing of large operand data sets. In some cases, the current memory resources do not perform well or are inadequate for the size of these data sets. These size and performance shortfalls could, in many cases, be overcome by performing Direct Memory Accesses (DMA) to and from memory.

The SRAM module provides a general-purpose memory block that the ColdFire processor can access in a single cycle. Because the SRAM module is physically connected to the processor's high-speed local bus, it can service processor-initiated access or memory-referencing commands from the debug module. The SRAM is dual-ported to provide DMA access. The SRAM is partitioned into two physical memory arrays to allow simultaneous access to both arrays by the processor core and another bus master.

Programmable Interrupt Timers (PITs)

- Four independent PITs
- Provides Interrupts at Regular Intervals
- Based on a 16-bit Free-running Down Counter
- Sets a Timeout Flag Upon Underflow
- Selectively Generate an Interrupt or Set Flag
- Timeout Period = 2 $^{PRE[3:0]}$ X (PM[15:0] + 1) System Clock Cycles
- Timeout Period is User Specified via a 16-bit Modulus Register
- Current Counter State Readable Anytime
- Can Continue to Operate in Low-power Modes
- Always Stopped in Stop Mode



Another module in the MCF5282 is the programmable interrupt timer (PIT).There are four programmable interrupt timers each of which generate interrupts at precise, regular intervals.

Each PIT module is based on a 16-bit free-running down counter.

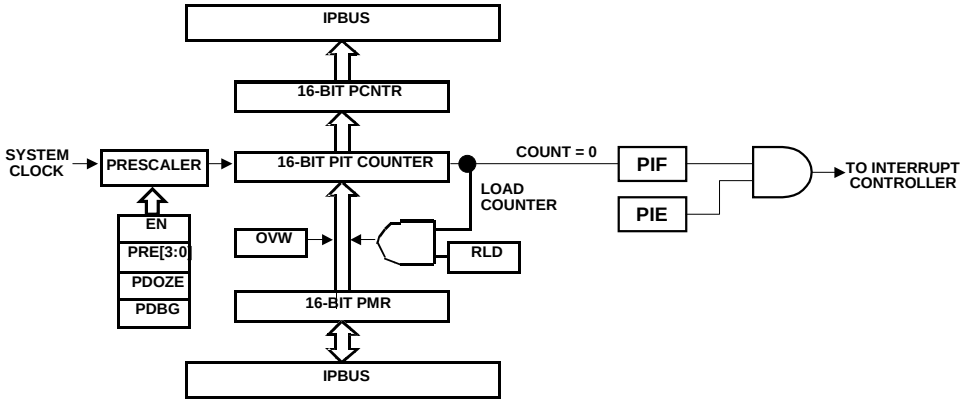
When the count reaches $0000, a timeout flag is set and the setting of this flag can trigger an interrupt if the PIT interrupt is enabled. The PIT timeout period is defined as the time it takes for the free-running down counter to reach zero.

The formula for this is timeout period is shown here.

The counter is initialized to whatever is programmed into the 16-bit modulus register, thereby giving the user full control over the timeout period. This timeout value given in terms of system clock cycles is a function of the prescaler and the modulus value, giving a maximum PIT timeout of two to the 31 system clock cycles. The Count register may be read at any time to check its current value.

A common application of the PIT is to bring the device out of a low-power state at regular intervals. The PITs are disabled in STOP mode.

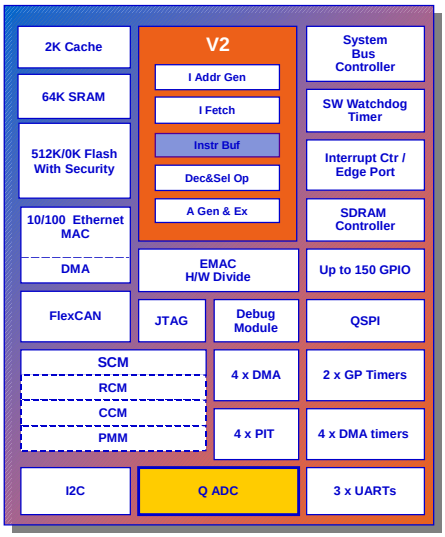
Programmable Interrupt Timers (PITs)



The programmable interrupt timer (PIT) is a 16-bit timer that provides precise interrupts at regular intervals with minimal processor intervention. The timer can either count down from the value written in the modulus register, or it can be a free-running down-counter. This device has four programmable interrupt timers, PIT1-PIT4.

QADC Module

- **10-bit Successive Approximation A/D**
- **Up to 8 A/D Channels Without External Multiplexing**
- **Signal Support for Up to Four 1-of-4 External Multiplexers**
- **Up to 18 A/D Channels With External Multiplexing**
- **Internal Sample and Hold with Programmable Sample Time**
- **Dual Command Queues (64 Entries) with Sub-queue Support**
- **Multiple Modes for Queue Initiating and Cycling**
- **Interrupt Capability for Queue Complete and Pause**
- **Selectable Result Formats.**



The Queued Analog to Digital Converter Module (QADC) in the MCF5282 is a 10-bit, uni-polar successive approximation A/D converter. The interface to the module consists of eight multi-function input/output pins, two reference voltage pins, and two power pins. There is built-in multiplexing and channel decode logic which can be enabled and used to reduce the number of analog inputs to the device. When multiplexing is deselected, up to eight channels can be individually fed in and read.

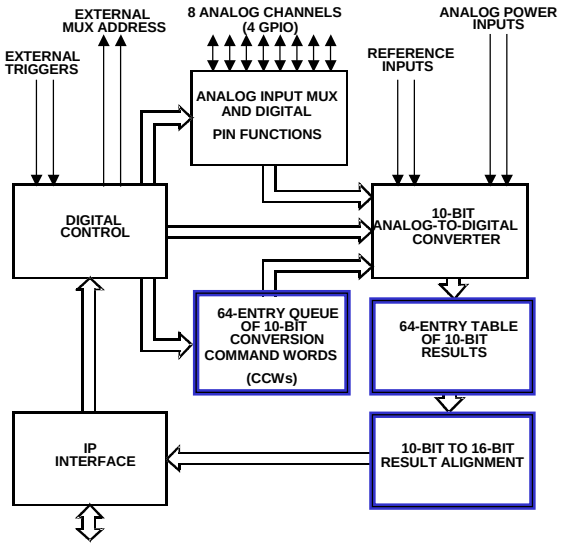
The channel select and device enable outputs of the device supports four 1-of-4 external multiplexers. Using the on-chip multiplexing support, up to 18 A/D channels can be read.

The internal sample and hold circuitry supports a sample time which is user programmable.

A sophisticated multi-level queuing system provides a high degree of flexibility in setting the order and frequency in which conversions take place. There is also built-in flexibility for initiating and terminating queue conversion operations. This control is supported with multiple interrupt capability.

Finally, the results can be read in one of three different selectable formats.

QADC Block Diagram



The block diagram for the QADC shows that eight pins are used for analog input. Four of these pins are in the bidirectional Port QA and the other four pins are from the bidirectional Port QB. Each of these eight pins have other functionality related to the QADC module, aside from their ability to be set as multiplexed or non-multiplexed analog input or digital I/O. Two of these functions are as external trigger input and external multiplexing control. The QADC also has a set of its own power pins as well as a set of high/low voltage reference pins.

The digital control block consists of a number of components including; control logic, the QADC clock, a periodic/interval timer, control and status registers, conversion command word and result table RAM. The control logic is used for conversion activities while the PIT is used for timed conversions. The control and status registers are used for mode selections and user control of the module. Control in this module allows for the setup of multiple queues of conversions and how each queue is triggered and terminated. The analog subsystem consists of multiplexing circuitry and an analog-to-digital converter. A state machine in this subsystem controls conversion sequencing while a successive approximation register and end-of-conversion signal generation control the timing.

Question

Is this statement true or false: The PIT counter can be either pre-loaded with a user-programmed value in the modulus register, or it can function as a free-running counter. Click the correct answer and Click Done.

A) True

B) False

Done

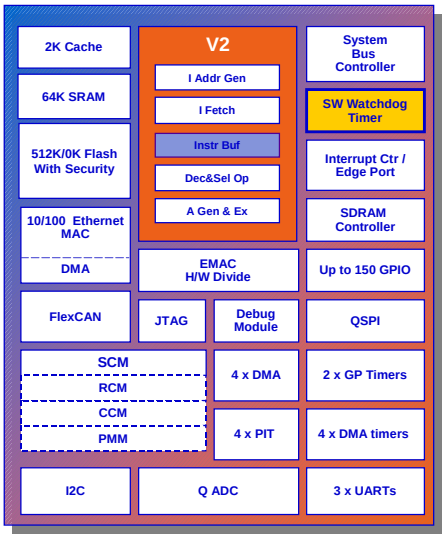
Consider this question about the ColdFire family of products.

Answer:

The PIT counter can be either pre-loaded with a user-programmed value in the modulus register, or it can function as a free-running counter.

Watchdog Timer

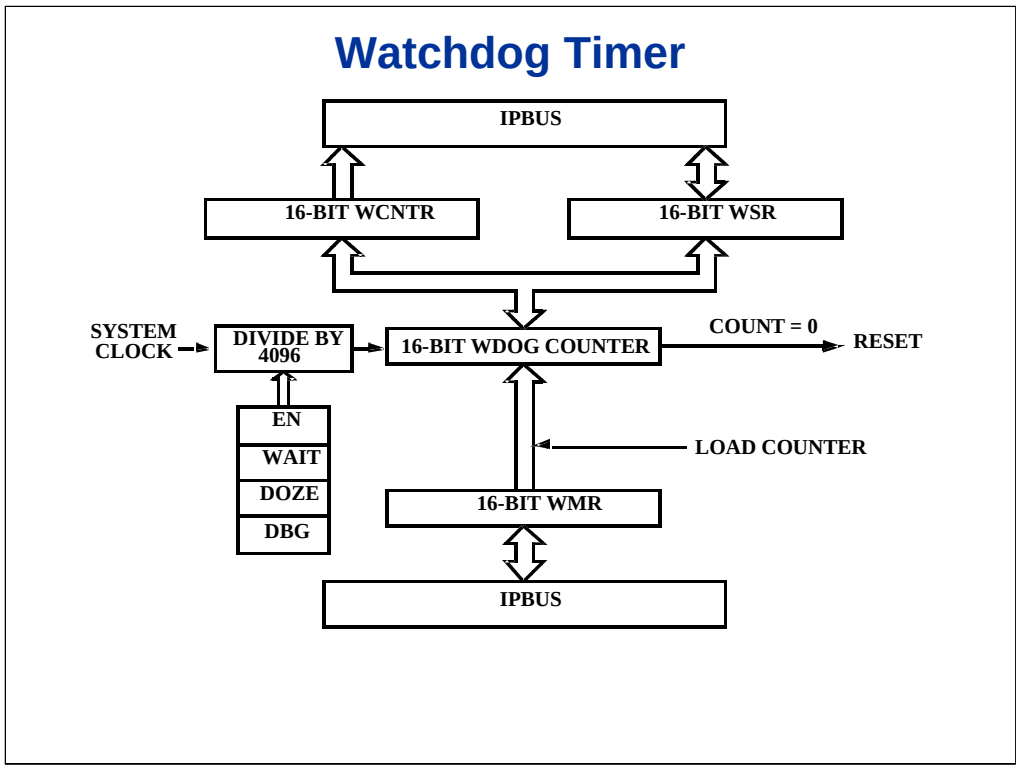
- **Used to Recover from Runaway Code**
- **Automatically Generates a Reset if Not Serviced**
- **Based on a 16-bit Free-running Down Counter**
- **Timeout Period is User Specified via a 16-bit Modulus Register**
- **Serviced by Writing Twice to the Service Register**
- **Current Counter State Readable Anytime**
- **Can Continue to Operate in Low-power Modes**
- **Two watchdog timers available on the MCF5282**



Now let's look at the ColdFire's watchdog timer. The watchdog timer is a 16-bit timer used to help software recover from runaway code. The watchdog timer has a free-running downcounter (watchdog counter) that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown by servicing the watchdog.

The Watchdog Control Register (WCR) contains four bits which are set to specify the operation of the watchdog module. The watchdog enable bit, EN , is set to enable the watchdog timer. This is a write-once bit and is set by default to enable the watchdog. The other three bits in this register, WAIT, DOZE, and HALTED, control whether the watchdog is operational during the other modes of operation--Wait, Doze and Halted modes. By default, all of these bits are set to stop the watchdog timer in these modes. The watchdog, if enabled, continues normal operation when coming out of one of these modes in which it was configured to stop. Note that the watchdog timer is always stopped in Stop mode.

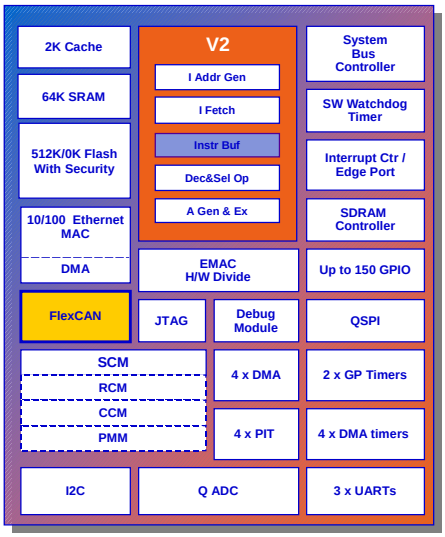
On the MCF5282, there are two watchdog timers that are available to the user. One provides compatibility with the one found on previous ColdFire devices and the other is described here.



The watchdog module is clocked by the system clock and is automatically prescaled by a factor of 4096. A free-running 16-bit down counter is used to cause a reset when its value reaches zero. The counter is prevented from reaching zero and causing a reset by the software writing to the Watchdog Service Register (WSR). The countdown can start at any 16-bit value programmed into the Watchdog Modulus Register. The value of the watchdog counter can be read at any time by reading the Watchdog Counter Register (WCR).

FlexCAN

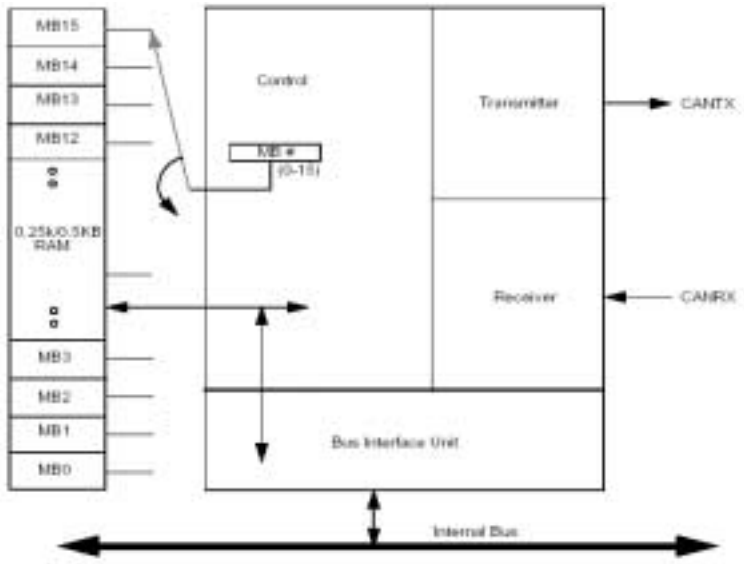
- **Full implementation of the CAN protocol specification - Version 2.0**
- **Programmable Bit Rate up to 1Mbit/sec**
- **Rx or Tx, all support Standard and Extended Messages.**
- **No read/write semaphores.**
- **Programmable transmit-first scheme: Lowest ID or lowest buffer number.**
- **Time Stamp, based on 16-bit free-running timer.**
- **Global network time, synchronized by a specific message.**
- **Programmable I/O Modes.**
- **Maskable interrupts**
- **Open network architecture**
- **Multimaster concept**
- **High immunity to EMI**
- **Short latency time for high-priority messages**
- **Low power sleep mode, with programmable wake up on bus activity**



Another module in the ColdFire V2 family is the FlexCAN module. It is a communication controller implementing the Controller Area Network or CAN protocol. It is based on and includes all existing TOUCAN module "superset". It is also a high speed (1 Mbit/sec), short distance, priority based protocol which can communicate using a variety of mediums (for example, fiber optic cable or unshielded twisted pair cable). The CAN protocol was primarily, but not only, designed to be used as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness, and required bandwidth.

The FlexCAN has a number of important features. First, it has our IP interface architecture. It also involves full implementation of the CAN protocol specification. It has Version 2.0 Flexible Message Buffers (up to 16 message buffers) of 0-8 bytes Data Length, each configurable as Rx or Tx. All of them support standard and extended messages. It also includes either 512 byte or 256 byte of RAM used for the message buffers.

FlexCAN Block Diagram



The module operation relating to message reception and transmission is identical to the TouCAN module. FlexCAN offers an increased number of RAM based message buffers (up to 16), all of which can be configured as either transmit or receive.This module can generate up to 19 interrupt sources (16 interrupts due to message buffers and three interrupts due to Bus-off, Error, and Wake-up).

FlexCAN & TouCAN Differences

FlexCAN	TouCAN
IP based interrupt structure	IMB3 based interrupt structure
Flexible message buffers	No Flexible message buffers
512 byte or 256 byte message buffer RAM	No message buffer RAM
Listen-only mode	No Listen-only mode

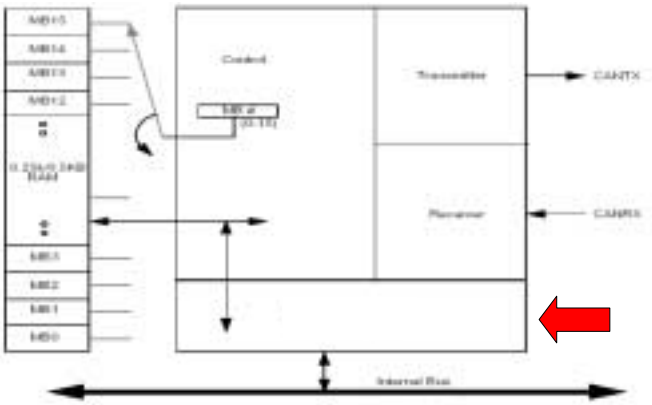
There are some significant differences between the FlexCAN and TOUCAN modules. The primary difference is in the interrupt structure. TouCAN uses an IMB3-based interrupt and FlexCAN uses an IP-based interrupt.

The FlexCAN module is flexible in that each one of its 16 message buffers can be assigned either as a Tx buffer or a Rx buffer. Each message buffer is also assigned an interrupt flag bit to indicate successful completion of transmission or reception, respectively. Note that for both processes, the first CPU action in preparing a message buffer should be to inactivate it by setting its code field to the proper value. This requirement is mandatory to assure proper operation.

Question

Which of the following is the name of the component of the FlexCAN block diagram that is indicated by the red arrow? Click the correct answer.

A) Bus Interface Unit
B) Flexible Message Buffer
C) Watchdog Control Register
D) Reset Controller



Consider this question about the ColdFire family of products.

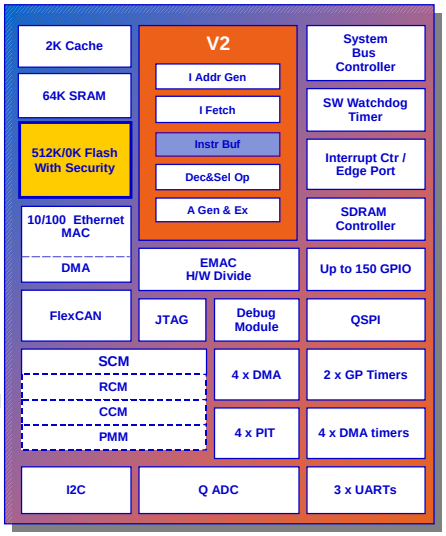
Answer:

The indicated component is the Bus Interface Unit.

ColdFire Flash Module (CFM)

Features

- 512 Kbytes of Flash memory
- Supports 66Mhz Flash array read operations with one wait-state access
- Concurrent program, erase or blank verify of all Flash array blocks
- Automated program and erase operation.
- Single power supply (MCF5282 Vdd) used for all module operations
- Read-while-write capability
- Optional interrupt on command completion
- Protection scheme to prevent accidental program or erase
- Access restriction control for supervisor/user and data/program space operations
- Security for single-chip operations
- Auto sense amplifier timeout for low-power, low-frequency operation read operations



Let's now turn our attention to the ColdFire Flash Module (CFM). This module is ideal for program and data storage for single-chip applications and allows for field reprogramming with no external high-voltage sources. The voltage required to program the CFM is generated internally by on-chip charge pumps.

The Flash Module itself is 512 kBs and supports read, write, and program/erase operations. It is possible to program or erase the entire flash array in a single operation or a user can program longwords or perform a 1 kB page erase. Also, a user can program a sector of flash while executing code from another. It supports 66 MHz flash array read operations with one wait-state access. It has concurrent program, erase or blank verify of all flash array blocks.

The CFM also contains a flexible protection scheme that will safeguard against accidental program and erase operations of the flash memory space to ensure that valuable data and code is not lost. There is also access restriction control for supervisor/user and data/program space operations.

One of the main features of the CFM is its security operation. This feature prevents unauthorized user access to the CFM during single-chip operation. Security can be bypassed in two ways in the event that a secured device needs to be re-accessed at a later time.

CFM Operation Modes

- **Normal Mode**
  - Read Operations
  - Write Operation
  - Program and Erase Operation
  - Page read verify
  - Stop Mode
- **Flash Protection**
  - Flash can be protected on a sector-by-sector basis
  - Protected sectors cannot be programmed or erased
- **Flash Security**
  - Forces chip into JTAG mode to prevent BDM reads of Flash
  - Back Door security override feature

In CFM Normal mode, the user can access the CFM registers and the CFM memory in order to perform operations such as read, program, erase, and blank check. The command sequence to perform flash operations is a simple three step process. The sequence is the same for erase verify, program, page erase, and mass erase operations. This allows for code sharing and shorter programs.

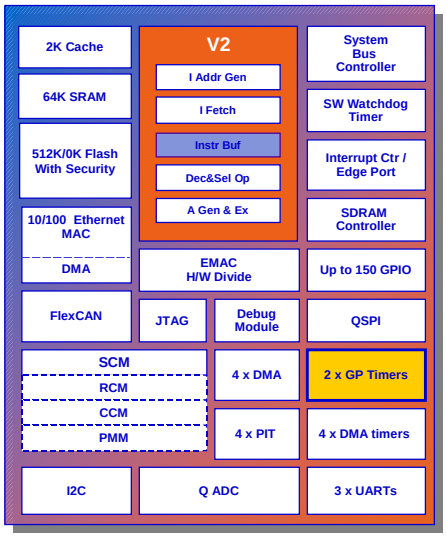
For power conservation, the device can enter stop mode. In this mode, the flash high voltage circuitry is switched off and any pending commands are aborted. The CFM array provides security information to the integration module and the rest of the MCU. A longword in the Flash configuration field stores this information. This longword is read automatically after each reset and is stored in the ColdFire Flash Module Security Register.

The CFM can also be put into a secured mode where unauthorized access to the module is prevented. This secured mode can be bypassed in two ways. First, an 8 byte back door comparison key can be programmed at a particular memory address within the flash array. During the back door access, data is written to this same location and if the data written is identical to the data already residing at that location, security is unlocked. Second, security can be bypassed by verifying that the CFM block is blank. If required, the mass erase command can be executed for each pair of flash physical arrays that comprise the block. The erase verify command must then be executed for all flash physical arrays within the block. If successful, then the CFM will be unsecured after the next reset.

General Purpose Timers (GPT)

Features

- Four 16-bit input capture/output compare channels
- 16-bit architecture
- Programmable prescalar
- Pulse widths variable from microseconds to seconds
- Single 16-bit pulse accumulator
- PWM capability using 2 channels with Toggle-on-overflow feature.
- External timer clock input



Finally, we'll look at the General Purpose Timers (GPT) of ColdFire. The MCF5282 has two 4-channel general purpose timer modules. Each consists of a 16-bit programmable counter driven by a seven-stage programmable prescalar. Each of the four timer channels can be configured to perform input capture or output compare. Additionally, one of the channels, channel three, can be configured as a pulse accumulator.

A timer overflow function allows software to extend the timing capability of the system beyond the 16-bit range of the counter. The input capture and output compare functions allow simultaneous input waveform measurements and output waveform generation. The input capture function can capture the time of a selected transition edge. The output compare function can generate output waveforms and timer software delays. Additionally, two channels can work together for pulse modulation capability. This capability can be made interactive for dynamically changing duty cycles or frequency control or it can operate continuously and without user intervention.

The 16-bit pulse accumulator can operate as a simple event counter or a gated time accumulator. The pulse accumulator shares GPT channel three when in event mode.

RTXC Quadros for ColdFire MCF5282

Features:

- RTXC Quadros Real Time Operating System Kernel
  - High performance with low latency
  - Small memory footprint (less than 50% of MCF5282)
- Networking Support
  - Core Internet Protocols
  - Application Level Protocol Servers
  - Application Level Protocol Clients

Three Versions with a Range of Pricing and Functionality

RTXC Quadros for MCF5282 **Special Edition**

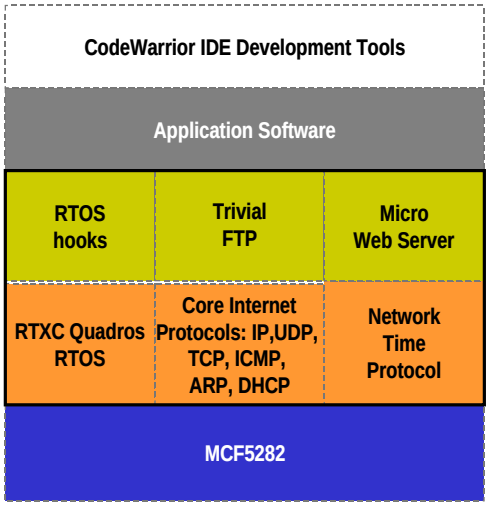
- FREE! (no NRE, no License, no Royalties)

RTXC Quadros for MCF5282 **Standard Edition**

- ~$20K License per Project

RTXC Quadros for MCF5282 **Professional Edition**

- ~$50K License per Project



A complete solution
for networked embedded control based on the ColdFire MCF5282, RTXC Quadros real-time operating system and CodeWarrior Development Tools for ColdFire, is designed to allow for ease of use and fast development by users of all experience levels.

In addition to the operating system, the software suite includes Ethernet Drivers for the MCF5282, Core Internet Protocols such as IP, UDP, TCP, ICMP, ARP and DHCP. It also includes application-level protocol servers, HTTP for small web servers, Trivial FTP servers for remote firmware updates and application level protocol clients for SMTP and SNTP. (SMTP provides the ability to send e-mail but not act as a relay server, while SNTP can retrieve current time information from a network NTP server)

Three versions of the software suite are available at a range of prices and functionality to meet the needs of all experience levels - from first time users to experienced users. The RTXC Quadros for MCF5282 Special Edition is Free and offers a fixed binary image that supports a limited number of tasks and network connections. This version is suitable for evaluation and prototyping and requires no NRE, license or royalties.

The Standard Edition is a configurable binary version providing flexibility in number of tasks, network connections and memory requirements. This is suitable for advanced embedded control and networking and is available for a license fee per project at approximately $20K.

Lastly, the Professional Edition is a fully configurable version with source code that supports a wide range of configuration options and code scaling. This package delivers optimal performance and design flexibility. This version is available for a license fee per project at approximately $50K.

Question

In the ColdFire General Purpose (GP) timers, which of the following channels can be configured as a pulse accumulator?
Click the correct answer and Click Done.

A) 1

B) 2

C) 3

D) 4

E) 5

Done

Consider this question about the ColdFire family of products.

Answer:

Channel three in the ColdFire General Purpose (GP) timers can be configured as a pulse accumulator.

Summary

- **MCF5249 Interrupt Implementation**
- **System Control Module (SCM)**
- **Edge Port (EPORT) module**
- **RAM Dual Port Processor**
- **Queued Analog-to-Digital Converter Module (QADC)**
- **Watchdog Timer**
- **FlexCAN module**
- **ColdFire Flash Module (CFM).**
- **General Purpose Timers (GPT) of ColdFire.**

In this module, ColdFire Application-Specific Peripherals, you learned the relationship between ColdFire and various application-specific peripherals. This provided you with a baseline of knowledge related to the ColdFire processor product line's integration.

In particular, you learned the features and operation of the following modules: the System Control Module (SCM), the Edge Port (EPORT) module, the RAM Dual Port Processor, the Queued Analog to Digital Converter Module (QADC), Watchdog Timer, the FlexCAN module, the ColdFire Flash Module (CFM), and the General Purpose Timers (GPT) of ColdFire.